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Memory Module Assembly Using Partially Defective Chips

Abstract of the Disclosure

Methods and devices for using less-than-perfect memory chips and packages in the manufacture of memory modules. In the preferred method the failed I/O lines in primary memory packages are disconnected and replaced by selected I/O lines from flawless or partially defective backup parts all mounted on the same module. The various processes comprise sorting of partially defective parts according to the results of wafer or packages test, judicious distribution of backup parts on a PC board module and routing of their I/O lines, optimized patching techniques and multi-level tests and repatching routines. The methods and processes are equally applicable to Chip On Board assemblies as well as package assemblies.